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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 200
TROY, MI 48098

EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	**PAPER NUMBER**
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/626,507	HO ET AL.	
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28, 44-63 and 79-105* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28,44-63 and 79-105* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/4/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to applicant's communication filed March 05, 2007 in response to PTO office action mailed December 04, 2006. The applicant's remarks and amendments to the claims and/or specification were considered with the results that follow.

2. In response to the last office action, claims 1, 6, 12, 16, 19, 21, 44, 51, 55, 58-59, 79, 90, 94, 96 and 98 have been amended. No claims have been added. Claims 29-43, 64-78 and 106-120 have been canceled. As a result, claims 1-28, 44-63 and 79-105 remain pending in this application.

3. Rejection of claims under 35 USC 112, second paragraph is withdrawn due to amendments filed on March 05, 2007.

4. Double Patenting rejection of claims with co-pending application 10/646289 have been withdrawn due to terminal disclaimer filed in later filed application (10/646289) on March 05, 2007.

Response to Arguments

5. Applicant's arguments with respect to claims 1-120 have been considered but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

6. The information disclosure statement (IDS) submitted on January 04, 2007 had considered by the examiner.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, 11,13-15, 20, 44-48, 50, 52-54, 79-83, 89, 91-92, and 97 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Zaidi et al. (US 6,601,126 B1) (Zaidi herein after), Jim Handy (The Cache Memory Book, second edition, published 1998) (Jim herein after), Taylor et al. (5,699,551) (Taylor herein after) and Jeddeloh (US 7,133,972).

As per claims 1, 44, 50 and 79, Zaidi teaches a cache control system (fig. 1) that controls data flow between a line cache (fig, 1, item 126), a first central processing unit (CPU) (fig. 1, item 110) and first and second memory devices (fig. 1, items 106 and 108), comprising:

a first line cache interface that is associated with the first CPU (taught as cache and channel controller interface the CPU bus, column 4, lines 39-41), that receives a

first program read request from CPU and that generates a first address from said first program read request (column 23, lines 30-32);

a first memory interface that communicate with first memory device and second memory interface that communicates with the second memory device (figs. 21-23, two memory devices, flash and SDRAM are connected to memory bus through MAC, which teaches first and second interfaces connected to first and second memory devices);

a cache that receives address that includes memory select portion; and a switch that selectively connects said line cache to one of said first and second memory interfaces (fig. 1, item 126 is a cache and even though it is explicitly not taught, when CPUs are provided with cache, CPUs initially try to access data from cache, thus cache receives address, column 23, lines 31-34 and lines 41-45, taught as CPUs supply a request and an address, the address includes both the port, device or memory bank address [memory select portion] and the requested memory location address. Referring figs. 20-23, col. 23 lines 22-29, "switched channel memory controller" allows multiple DMA (and processors) to simultaneously communicate with multiple output channels. Also, col. 23, lines 40-45, suggests that CPU bus can be connected to an external flash memory through one channel and SDRAM through another channel. These statements clearly state there are separate and selective communication interfaces between the connections, figs. 21, 22 and 23 shows separate lines are connected to the memory interfaces). **(switch providing separate/distinct interfaces are known in the art, because a separate and independent interface avoids bus or memory bank conflict and hence increases the speed of the system [motivation to use switch], see Jeddeloh US 7,133,972, fig. 3, col. 4, lines 30-64, presented as an evidentiary reference).**

Zaidi explicitly fails to teach line cache receiving first address and comparing address to stored addresses and if match occurs it returns data to CPU, and retrieves data from one of the first and second memories if miss occurs, but a system with processor and cache memory is well known to one of ordinary skill in the art at the time of invention, and when CPU issues read request in such a system, cache compares the address with the stored addresses and returns the data to CPU and if miss occurs it retrieves data from higher latency storages (Jim, page 42-43, section 2.1.3) (also applicant's admitted prior art in the background of the invention section).

Zaidi teaches sending first address with bank (memory) select portion and memory location address (Zaidi, col. 23, lines 31-34) but fails to teach sending a second address based on first address. Taylor teaches computer systems using physical cache, which requires address translation occurring before the cache access (cache receiving translated/second address based on first address) (Taylor, column 1, lines 26-40). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize physical cache as taught by Taylor in the system of Zaidi and Jim because virtual memory provides protection, large address space and physical cache memories are simpler to build (Taylor, column 1, lines 26-40).

Zaidi, Jim and Taylor explicitly fail to teach the limitation "wherein said switch includes a plurality of selectors that each receives the second address and each select between first and second sets of signals relating to the first and second memory devices, respectively based on the second address". However, Zaidi teaches CPUs connect to either SRAM or flash memory through switched channel memory controller

as explained above, and the selection of respective signals are inherent in the system of Zaidi, because it is well known at the time of the invention to one having ordinary skill in the art that the signals (such as clock and request and acknowledgement etc.) are required for proper communication to be occur between the processor and cache or between cache and lower level storage systems (**see Jeddeloh, col. 4, lines 8-29, "the memory hub (switch) includes a processor interface 150 that is coupled to the processor 104 through a plurality of bus and signal lines, as is well known in the art". Jeddeloh, col. 4, lines 56-67, "for example, the switch 160 may be a cross-bar switch that can simultaneously couple at the processor interface and the memory interfaces 170a-c to each other. The switch can also be a set of multiplexers (plurality of selectors)"**).

As per claims 2-3, 45-46 and 80-81, Zaidi teaches that the first memory device is RAM (fig. 1, item 108).

As per claims 4, 47 and 82, Zaidi teaches the second memory device is flash memory (fig. 1, item 106).

As per claim 5, 48 and 83, Zaidi teaches the first CPU is an advanced risc machine (ARM) processor (column 5, lines 35-36).

As per claims 11 and 89, Zaidi teaches a cache memory as per claim 1 and memories are used for storing data. Zaidi fails to teach cache with a Content Addressable Memory (CAM). Jim teaches a cache memory with CAM, which stores addresses associated with data stored in the cache memory (page 14, sec. 1.5, page 15, fig. 1.7). Jim teaches determining when hit and miss occurs and retrieves data from higher latency memories (first and second memories) when miss occurs (Jim, pages 42-

43, sec. 2.1.3 and pages 46-47, fig. 2.4). Thus Jim inherently teaches cache state machine.

It would have been obvious to one having ordinary skill in the art at the time of invention have used Zaidi's dual processor system and modified to use the cache with CAM as taught by Jim because CAM permits content of memory to be searched and matched instead of having to specify a memory location in order to retrieve data from memory (Jim, page 14, sec. 1.5). This allows data to be stored at any location in a cache (Jim, page 16, paragraph 3)

As per claims 13-14, 52-53 and 91-92, Jim teaches a cache replacement algorithm Least Used Page, which replaces least used page with data retrieved form the first or second memory when miss occurs (page 57, paragraph 2, page 61, pars. 3-4). Thus Jim inherently teaches least used page device.

As per claims 15 and 54 Jim teaches that state transitions of cache state machine are based, in part on at least one internal state of the CPU (page 42, paragraph 2 and 3 and sec. 2.1.3)

As per claims 20 and 97, Jim teaches that cache can have many ways of implementations depending upon the address bits used in the system (page 54, paragraphs 2 and 3). Thus Jim inherently teaches cache with 4 pages of 8 x 32.

9. Claims 16-18, 55-57 and 93-95 are rejected under **35 U.S.C. 103(a)** as being unpatentable in view of Zaidi, Jim Handy, Taylor and Jeddeloh and in further view of Bryant et al. (4,008,460).

Claims 16-18 are similar in scope with combination of claims 1, 11, 13 and 14. Zaidi, Jim Handy, Taylor and Jeddeloh teach all the limitations of claim 16, including identifying first least used page and replacing first least used page in case of cache miss (limitation of claim 17) but fail to teach identifying first and second used page and replacing second least used page (claim 18). Bryant teaches identifying first and second least used page and replacing second least used page (Bryant, col. 3, lines 52-57).

It would have been obvious to one having ordinary skill in the art at the time of the invention to utilized first and second least used page replacement method as taught by Bryant in the system of Zaidi, Jim Handy, Taylor and Jeddeloh to avoid wrap-around delay associated with LRU policy and increase system performance (Bryant, col. 2, lines 7-16, lines 43-46).

Claims 55-57 and 93-95 are rejected under same rationales as applied to claims 1, 11, 13-14 and 16-17.

10. Claims 6, 21-24, 28, 49, 59-63, 84, 98-101 and 105 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Zaidi, Jim Handy, Taylor and Jeddeloh as applied to claims 1-5, 11, 13-15, 44-48 and 79-83 above, and further in view of Barroso et al. (US 6,725,334 B2).

As per claims 6, 49 and 84, Zaidi and Jim teach a dual processor system with two caches (fig. 2, items 202 and 214, first and second processors, and items 208 and 224, two caches). Zaidi, Jim and Taylor inherently teach cache interface with first and second CPUs and both generates read requests and hence first and second address as taught in claim 1. Zaidi teaches system with two second level caches for two processors but fails to teach cache arbitration device which communicates with first and second cache interfaces and resolves cache access conflicts between first and second CPUs. Barroso teaches a second level cache with switch (fig. 1, item 130 and 120), which provides interfaces with first and second CPU and arbitrates between first and second CPU (column 4, lines 10-21) (**switch providing separate/distinct interfaces are known in the art, because a separate and independent interface avoids bus or memory bank conflict and hence increases the speed of the system, see Jeddeloh US 7,133,972, fig. 3, col. 4, lines 30-64, presented as an evidentiary reference**).

It would have been obvious to one having ordinary skill in the art at the time of invention would have modified the multiple cache with multiple processor system of Zaidi and used one cache with switch as taught by Barroso to reduce the cost and the waste of the cache capacity (column 1, lines 45-65).

Claims 21-24, 59-63, 84, 98-101 and 105 are similar in scope with combination of claims 1-6, 11, 13-15 and hence rejected under same rationales as applied to claims 1-6, 11 and 13-15 above.

11. Claims 7-10, 25-27, 85-88 and 102-104 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Zaidi, Jim Handy, Taylor, Jeddeloh and Barroso as applied to

claims 1, 6, 11, 13-14, 16-17, 44-48 and 79-84 above, and further in view of Alexander et al. (6,131,155).

As per claims 7-8, Zaidi, Jim Handy, Taylor, Jeddeloh and Barroso teach all the limitations of claims 1-6 above but fail to teach direct interfaces from CPUs to memory devices. Alexander teaches CPU programmed to accessing main memory directly, bypassing cache access (Alexander, abstract).

It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize the direct access interface to memory, bypassing the cache as taught by Alexander in the system of Zaidi, Jim Handy, Taylor, Jeddeloh and Barroso, because data caches provides performance improvement only if program execution performs repeated accesses of data over a short period of time to a small group of data and large amounts of data transfers degrades the performance, so bypassing a cache and directly reading data from memory increases the performance (Alexander, abstract, col. 2, lines 21-56). Also providing a direct and independent interface avoids bus or memory bank conflict as explained with respect to claims 1 and 6 above.

As per claim 9, Zaidi and Barroso teach an arbiter and MAC (Zaidi, fig. 2, items 242, 244) and switch (Barroso, fig.1, item 120) to resolve memory access conflict (Zaidi, column 23, lines 40-45) but fail to teach arbiter for direct read/write interface. It would have been obvious to one having ordinary skill in the art at the time of the invention would provide arbiter for direct (bypassing cache interface) interface, because when multiple CPUs accessing memory device providing arbitration avoids the conflict for same data.

As per claim 10, Zaidi teach an application specific integrated circuit (ASIC) which can be used to provide interconnection structure and method for efficient integration variety functional circuits (Zaidi, column 2, lines 63-65): It would have been obvious to one having ordinary skill in the art at the time of invention have used the embedded system of Zaidi to control the hard disk drive and its components for better performance and compact design.

Claims 25-27, 85-88 and 102-104 are rejected under same rationale as applied to claims 7-10 as above.

12. Claims 19, 58 and 96 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Zaidi, Jim Hardy, Taylor, Jeddeloh and Barroso and further in view of Veidenbaum et al. (Adapting Cache Line Size to Application Behavior, pub. 1999).

Claims 19, 58 and 96 are similar in scope with combination of claims 1-6 above. But the combination of Zaidi, Jim, Taylor, Jeddeloh and Barroso fail to teach selecting size of the cache line based on application running. Veidenbaum teaches adapting cache line size according to application running (Veidenbaum, abstract).

It would have been obvious to one having ordinary skill in the art at the time of the invention to use cache line size based on application running as taught by Veidenbaum in the system of Zaidi, Jim, Taylor, Jeddeloh and Barroso to improve miss rate and memory traffic (Veidenbaum, abstract).

13. Claims 12, 51 and 90 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Zaidi, Jim Hardy, Taylor, Jeddeloh and Barroso and further in view of Ebner et al. (US 6,928,525).

Claim 12 is similar in scope with combination of claims 1-6 and Zaidi, Jim Hardy, Taylor, Jeddeloh and Barroso teach all the limitations, but they combined failed to teach accessing one page by one of first and second CPUs, while other of first and second CPUs is accessing another page. Ebner teaches shared cache memory, which allows multiple simultaneous access to data held in different cache lines of cache (Ebner, Abstract). It would have been obvious to one having ordinary skill in the art at the time of the invention to utilize shared cache allowing multiple simultaneous access to different lines of cache as taught by Ebner in the system of Zaidi, Jim Hardy, Taylor, Jeddeloh and Barroso to improve system performance by allowing concurrent accesses to cache lines (Ebner, col. 2, lines 32-39).

Claims 51 and 90 are also rejected under same rationales as applied to claim 12.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

kmp

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
4-2-07